Claims

1. Storage device for a multibus architecture, comprising

– at least one memory (M) to store data (d), information and/or addresses,

– a memory connection (B) including a port (B0) to connect the memory (M) to a first bus (D0) of a multibus architecture (P, D0, D1, R),

– wherein the memory connection (B), the port (B0), and the first bus (P) have data lines (DL) to transmit the data (d), and, as required, transmit addresses (a) and/or control information to control the memory (M),

characterized by

– a switching device (SW, MTR, CU, ARB, MOD) to selectively connect the memory connection (B) to one of the buses (D1, P, R) for a memory access to effect transmission of data, addresses, and/or control information from or to this bus.

2. Storage device according to Claim 1, comprising a memory-specific logic device (L) and an interrupt line (STL) to transmit an interrupt signal (st) to a processor system (PU) so as to control the complete system such that by sending the interrupt signal (st), an interruption of the processor operation is always triggered for one clock cycle whenever a memory access is to be effected by the memory (M) to two different buses (P, D0, D1, R), or to the memory (M) by these buses, within two successive clock cycles.

3. Memory according to Claim 1 or 2, comprising an analyzer (ARB, CU) connected on the input side of the memory (M) for analyzing addresses on the address lines (AL) assigned to the buses and/or the memory for memory accesses, and for

appropriately switching the switching device (SW) to one of the corresponding buses (P, D0, D1, R).

4. Storage device according to Claim 3, wherein the analyzer (ARB, CU) is designed for analyzing a part of the addresses, and for switching and assigning a memory access for address segments smaller than the word width of a bus transmitting the addresses or of the address lines (AL).

5. Storage device according to Claim 3 or 4, comprising an adjustable separator device, specifically a programmably adjustable separator device (MTR) to store a memory address of the memory (M) for analysis by the analyzer (ARB, CU).

6. Storage device according to one of Claims 3-5, wherein the analyzer has a common access control device (ARB) to switch the switching device (SW), and one comparator (CU) each per bus (P, D0, D1, R) to compare the address with the memory address of the memory (M).

7. Storage device according to one of Claim 3-6, wherein the analyzer has a modifier (MOD) which is designed to process different data types and/or access types which are applied to the modifier (MOD) and/or to a data memory segment of the memory (M) through data lines, subaddress lines, and/or access signal lines (DL, SAL, ACL) selected by the switching device (SW) in order to transmit states on the bus lines (DL).

8. Storage device according to one of the foregoing claims, comprising a or the logic device (L, CU) to issue a block loss signal (BM) through a loss line (BML) to a

higher-level processor system (PU) in response to a deviation from the announced and executed data transfers during the memory access.

9. Storage device, comprising a plurality of storage devices according to a foregoing claim which is switchably connected to one bus each within a multibus architecture having a plurality of busses (P, D0, D1, R).

10. Storage system according to Claim 9, which – particularly in the case of a switch between read access and write access for one of the memories (M) – is designed to effect the clock-cycle-based alternating control of different memories (M) by a common high-level processor system (PU).

11. Processor, including at least one storage device according to one of Claims 1-8, or a storage system according to Claim 9 or 10, as the processor memory.

12. Method of operating a storage device according to one of Claim 1-8, or a storage system according to Claim 9 or 10, wherein
– a memory connection (B) is selectively connected by a switching device (SW) to one bus (P) of a plurality of buses (P, D0, D1, R) through which data information, address information, and/or control information is subsequently transmitted.

13. Method according to Claim 12, wherein an interrupt signal to suspend the processor clock of a higher-level processor (PU) is generated and issued by a memory-specific logic device (L) whenever a memory access by the memory to two different buses, or a memory access by two buses to the memory, is to take place within two successive clock cycles.

14. Method according to Claim 12 or 13, wherein address lines assigned to the memory for memory accesses on the buses, or separate address lines to determine the switching position of the switching device, are analyzed in a logic device (L) on the input side of the memory (M).

15. Method according to Claim 14, wherein address segments smaller than the word width of the address are searched during the analysis as the assigned memory address, then used as the switching criterion.

16. Method according to Claim 14 or 15, wherein the highest-value bit of the address is compared with an adjustable register, specifically a programmable adjustable register (MTR) to determine the access address, and the memory access is then enabled only in the case of a match.

17. Method according to Claim 16, wherein to implement an overlay procedure another memory, specifically a slower and larger memory, is overlaid.

18. Method according to one of Claims 12-17, wherein to control the switching device (SW) selected data lines, subaddress lines, and/or access signal lines of a selected bus are used to generate switching signals and commands in the event data or information transmitted through the selected bus do not match, in terms of the amount of data, the amount of available memory space per memory access operation.

19. Method according to one of Claims 12-18, wherein to prevent a collision between memory accesses a command is generated by the processor either in the form of a clock control signal to interrupt the processor clock or in the form of a memory selection signal to select a different storage device, and is then sent to the processor (PU).